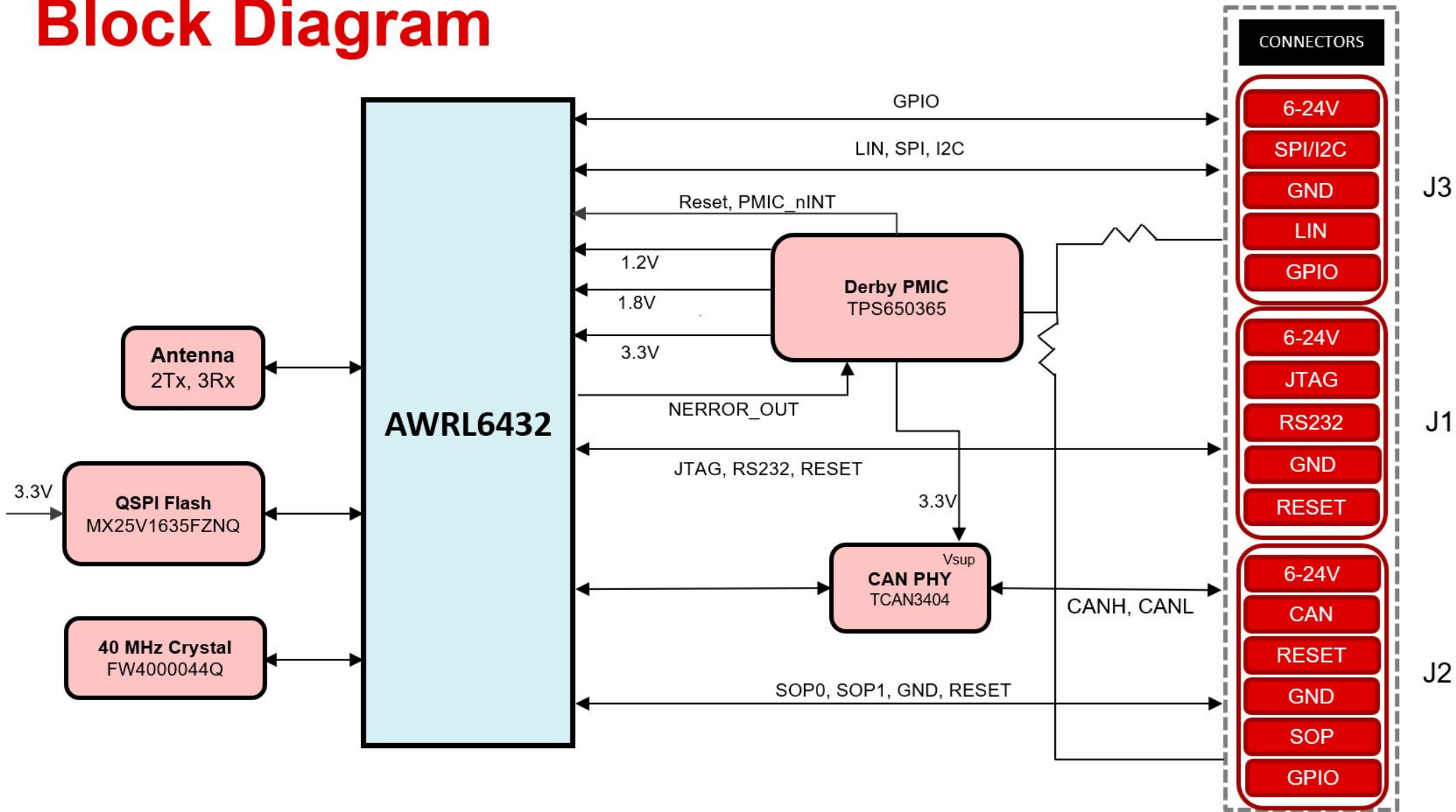


| Revision History | | | | |
|------------------|-------|---------------|-------------|-------|
| Rev | ECN # | Approved Date | Approved by | Notes |
| | | | | |

BLOCK DIAGRAM

Block Diagram



Texas Instruments and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. Texas Instruments and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. Texas Instruments and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

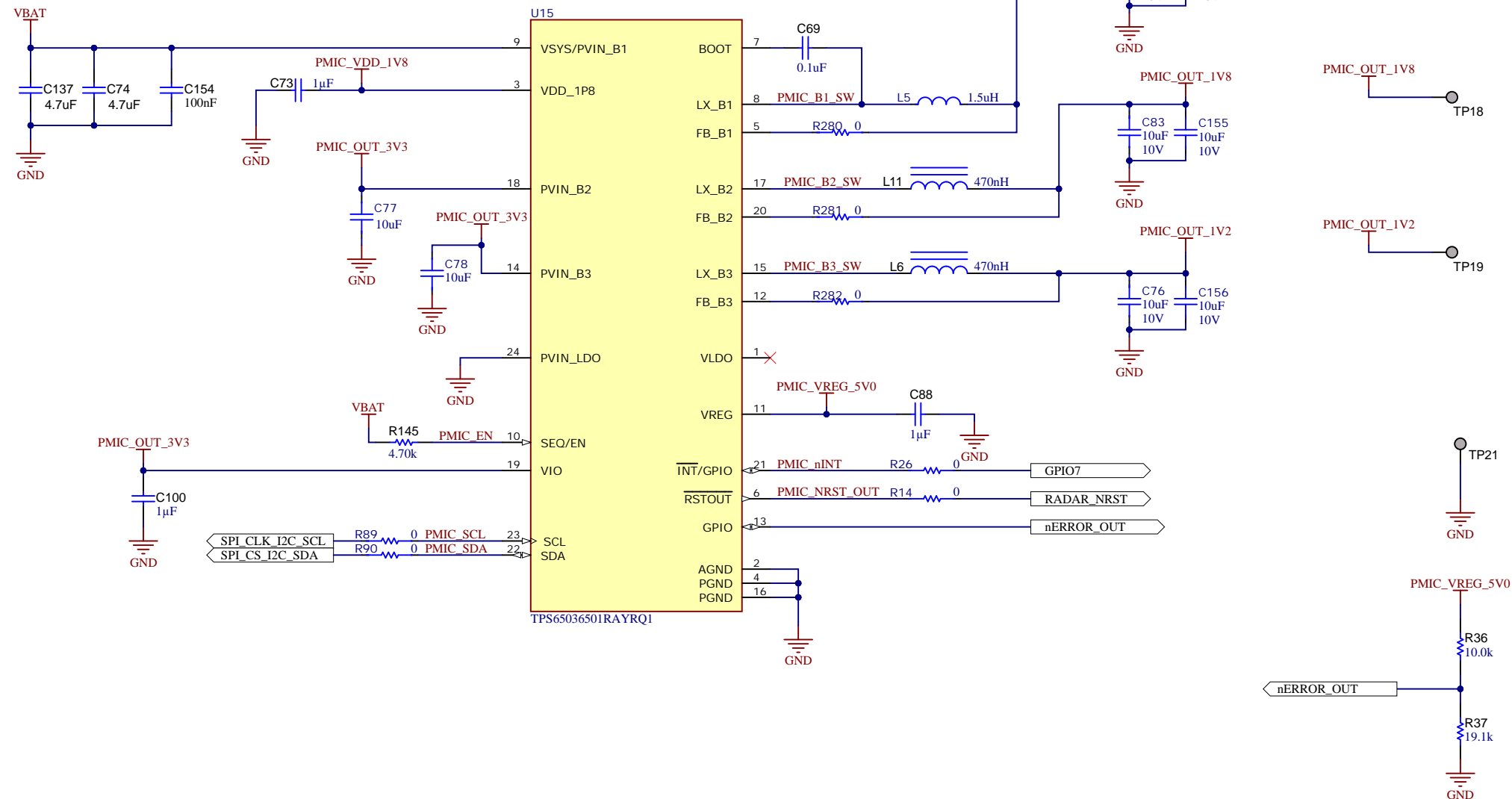
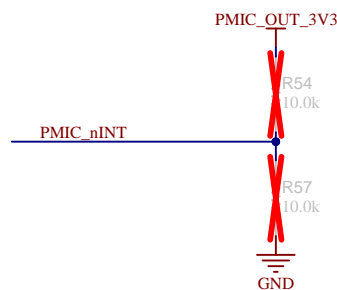
| | | |
|--|---|---|
| Orderable: AWRL6432InCabinRefDes | Designed for: Public Release | Mod. Date: 8/22/2024 |
| TID #: TIDEP-01037 | Project Title: AWRL6432_INCABIN_REF_DESIGN | |
| Number: TIDEP-01037 Rev: A | Sheet Title: BLOCK DIAGRAM | |
| SVN Rev: 3736 | Assembly Variant: 001_AWR | Sheet: 1 of 7 |
| Drawn By: Mistral | File: AWRL6432_REF_DESIGN_Block_Diagram.Sch | Size: B |
| Engineer: Mistral | Contact: http://www.ti.com/support | |

| | | | | | |
|---|---|---|---|---|---|
| 1 | 2 | 3 | 4 | 5 | 6 |
| A | | | | | A |
| B | | | | | B |
| C | | | | | C |
| D | | | | | D |

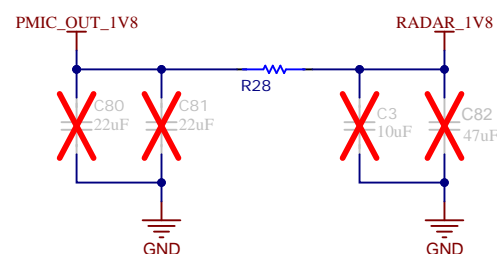
TABLE OF CONTENTS

| SHEET NO. | SHEET NAME |
|-----------|--------------------------------|
| 1 | BLOCK DIAGRAM |
| 2 | TABLE OF CONTENTS |
| 3 | PMIC |
| 4 | xWRL6432_CHIP |
| 5 | DECOUPLING_CAPS & QSPI_FLASH |
| 6 | CAN_PHY & INTERFACE_CONNECTORS |
| 7 | EVM_HARDWARE |

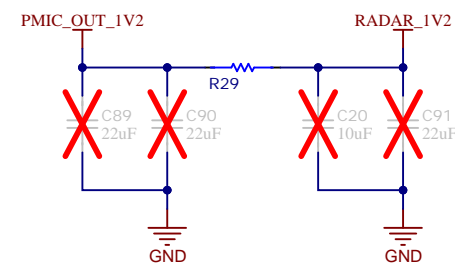
Texas Instruments and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. Texas Instruments and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. Texas Instruments and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.



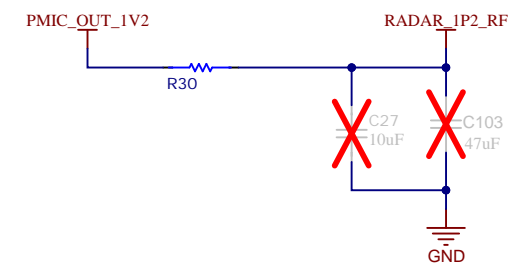
Design Note:
Alternate Inductor part for R31 is LQM2MPZR10MJHL



Design Note:
Alternate Ferrite bead part for R28 is MPZ2012S300ATD25



Design Note:
Alternate Ferrite bead part for R29 is MPZ2012S300ATD25

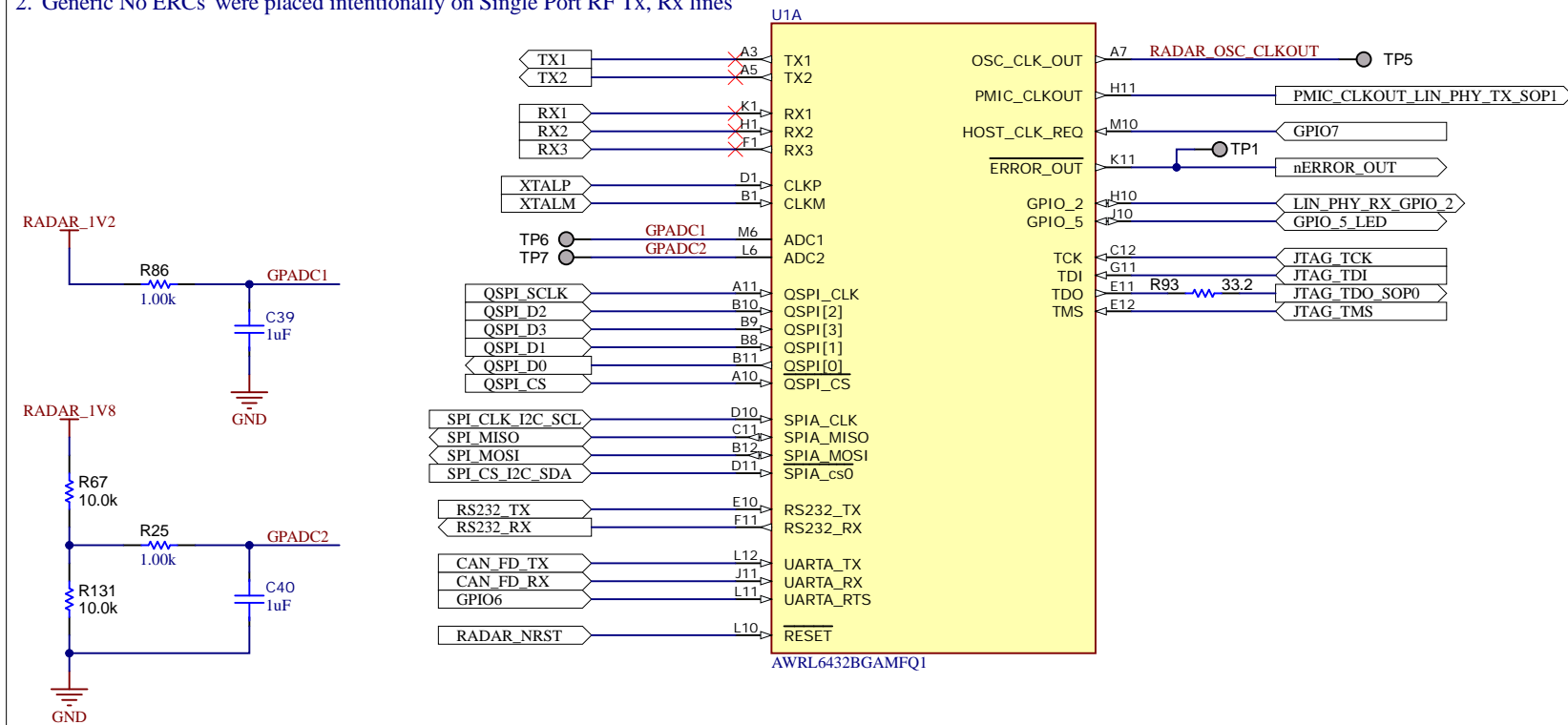


Design Note:
Alternate Ferrite bead part for R30 is MPZ2012S300ATD25

xWRL6432 CHIP - INTERFACES

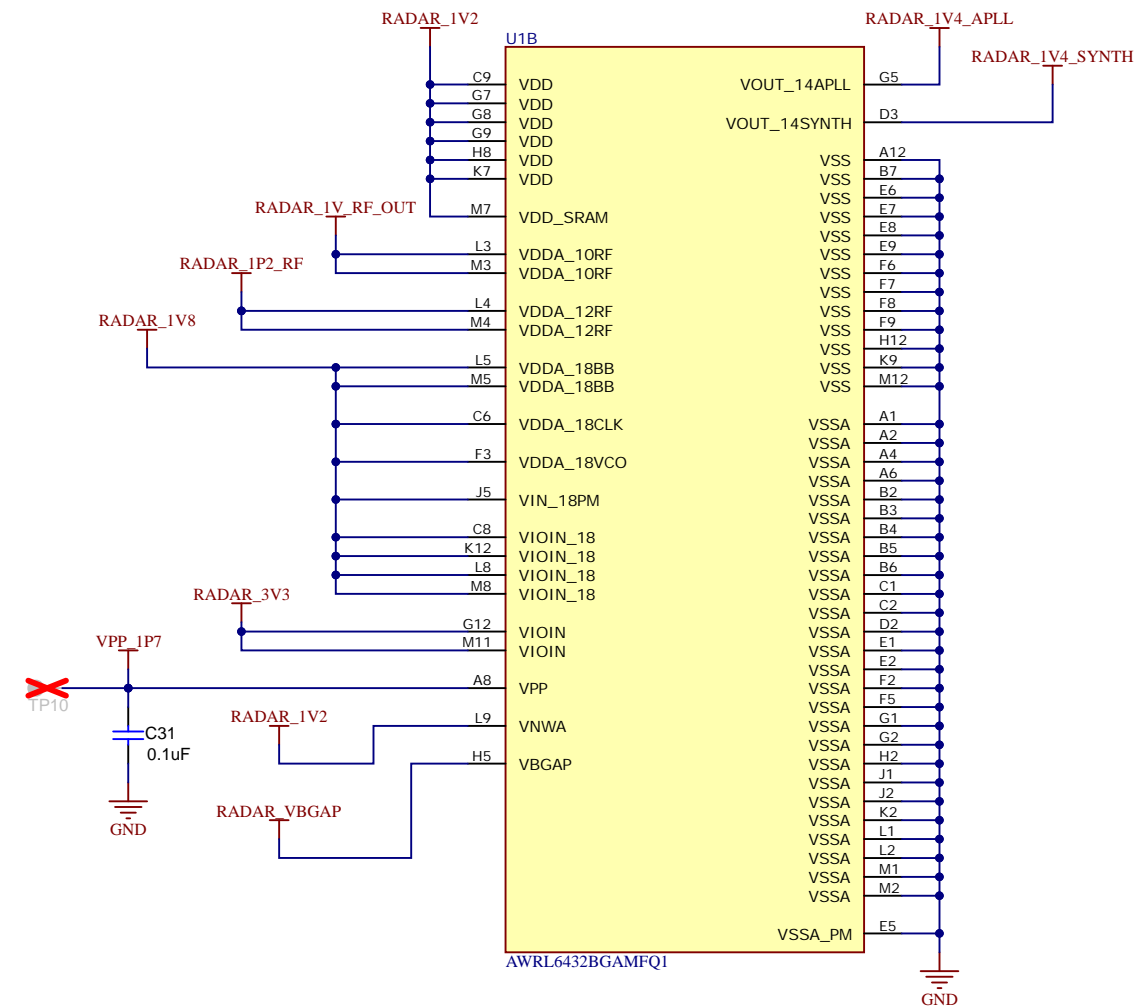
Design Note:

1. Antenna traces are GCPW traces
2. 'Generic No ERCs' were placed intentionally on Single Port RF Tx, Rx lines

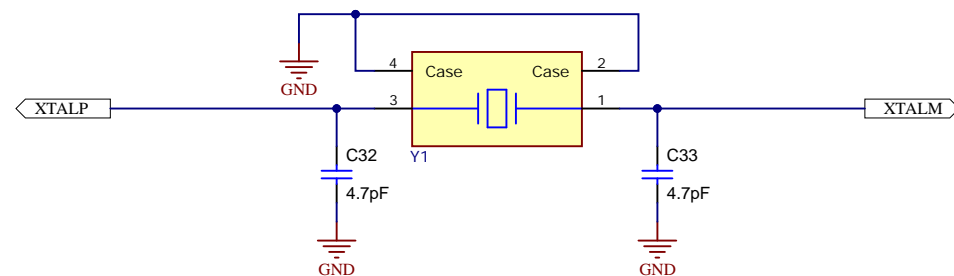


CAD Note: Place C39 and C40 close to AWRL6432 IC

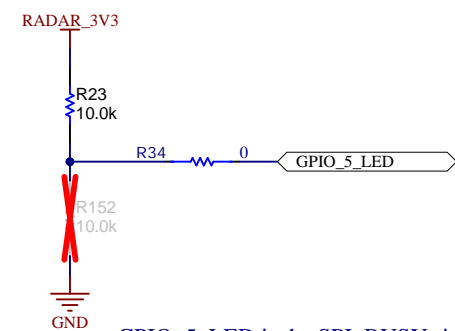
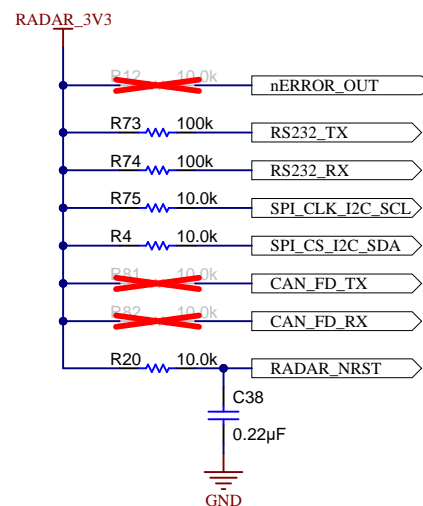
xWRL6432 CHIP - POWER



40 MHz CRYSTAL OSCILLATOR

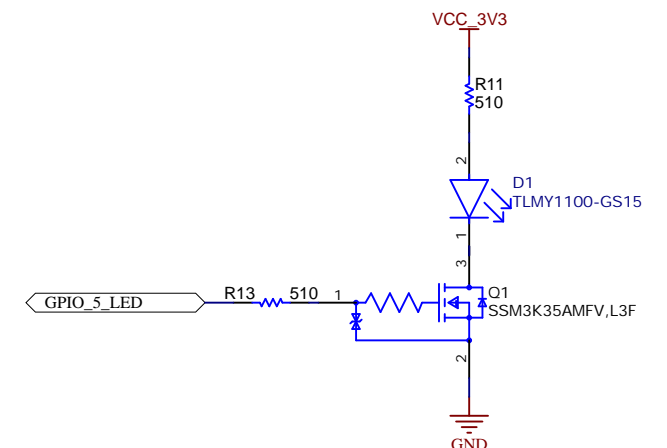


Alternate Crystal part number : CX2016SA40000D0PTWC1



GPIO_5_LED is the SPI_BUSY signal

USER LED



A

B

C

D

A

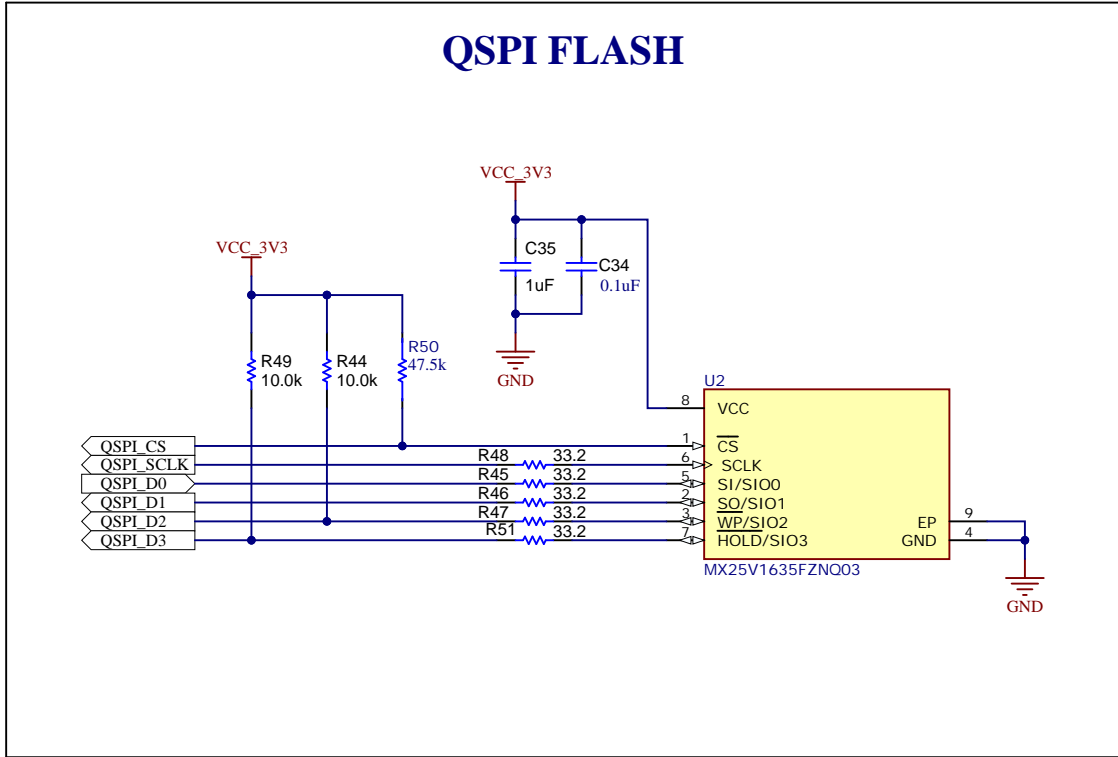
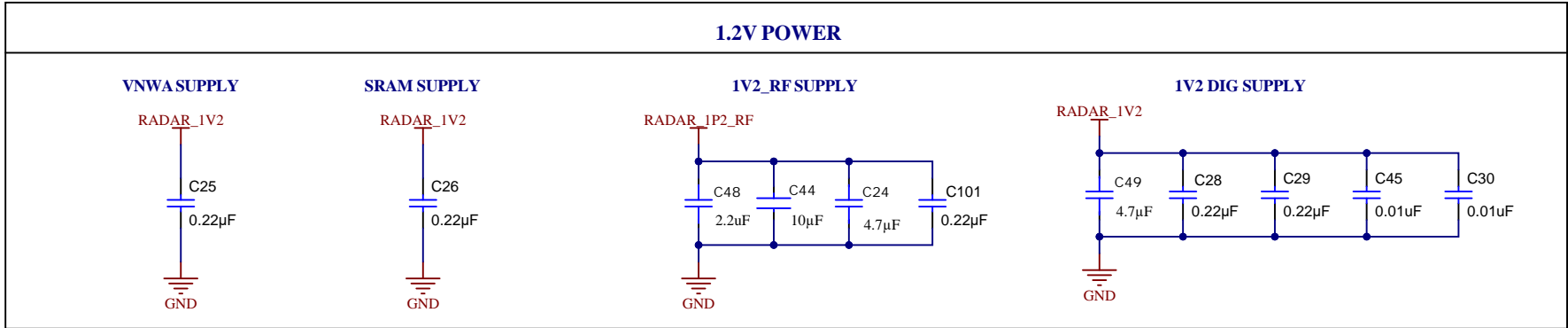
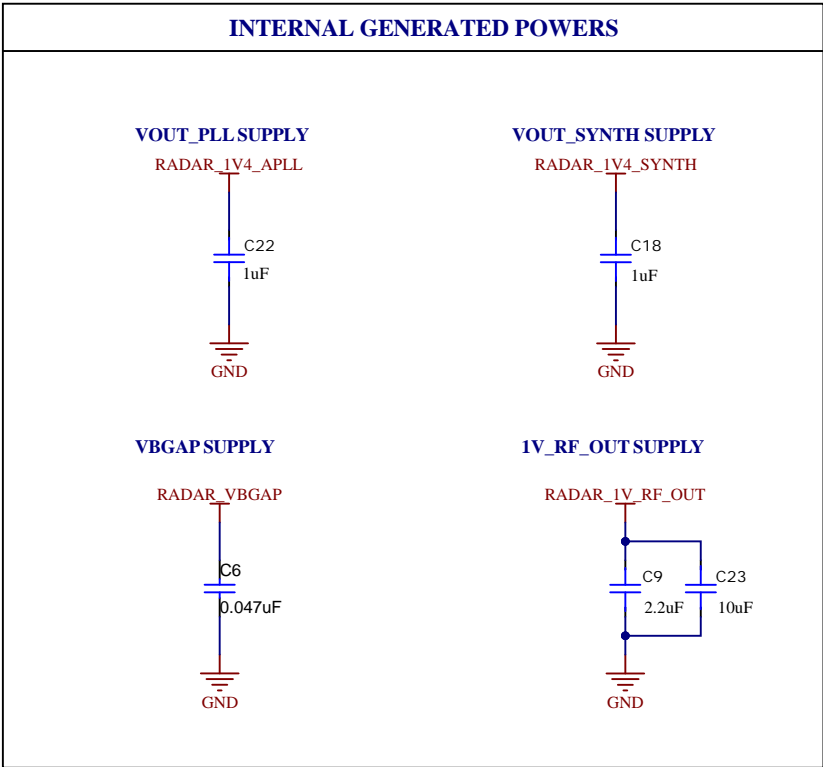
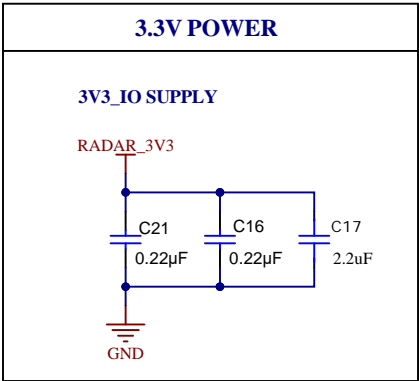
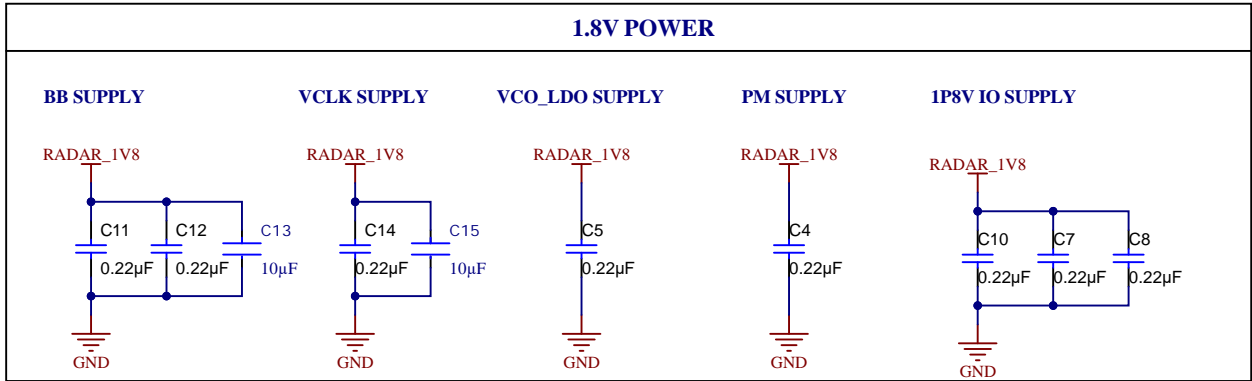
B

C

D

Review Note
T1 to review the Decap section
Let us know for any possible decaps optimization

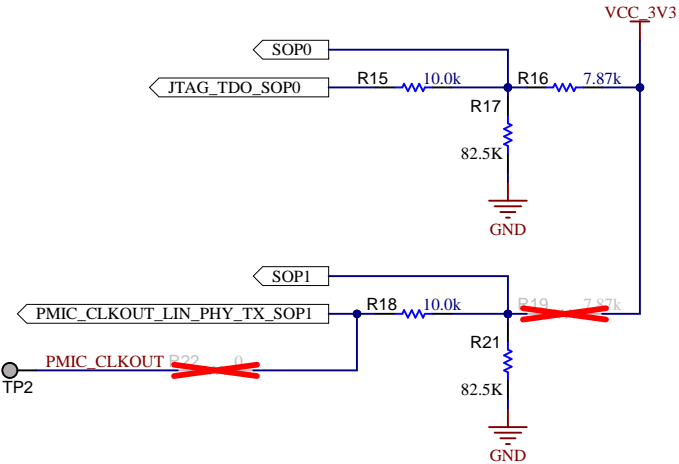
SUPPLY_DECOUPLING_CAPS



SOP0 & SOP1

| SOP CONFIGURATION | | |
|-------------------|--|-------------|
| SOP Mode | PMIC_CLK_OUT, TDO | SOP1 , SOP0 |
| SOP_MODE1 | Device Management Mode / QSPI flashing mode | 0 0 |
| SOP_MODE2 | Application Mode / Functional Mode | 0 1 |
| SOP_MODE4 | Debug Mode / mmWave Studio connectivity mode | 1 1 |

Design Note : Default SOP state is Functional Mode



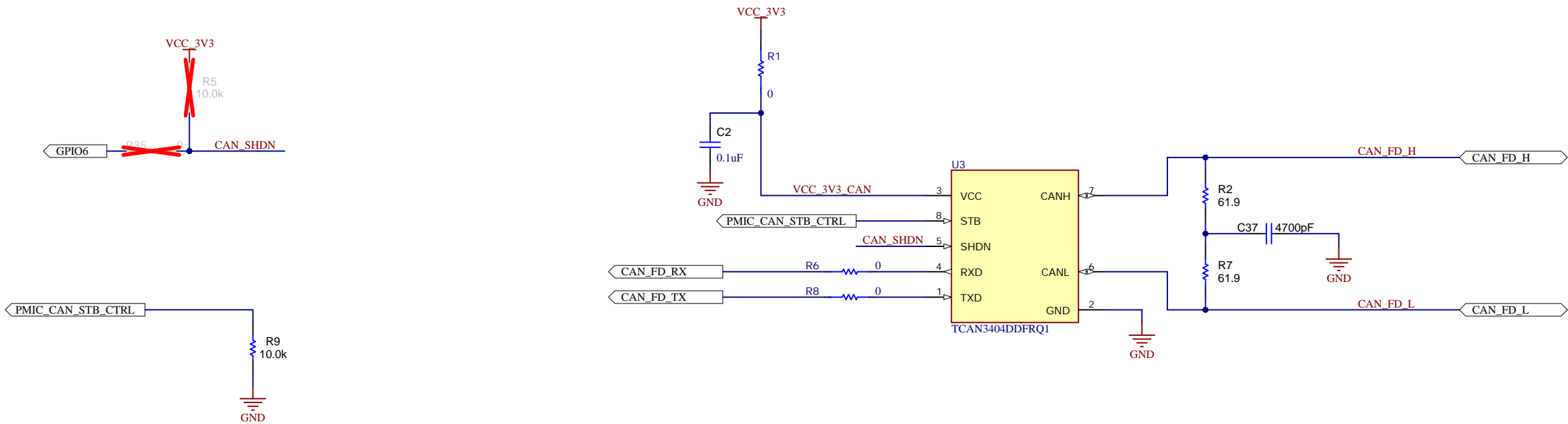
A

B

A

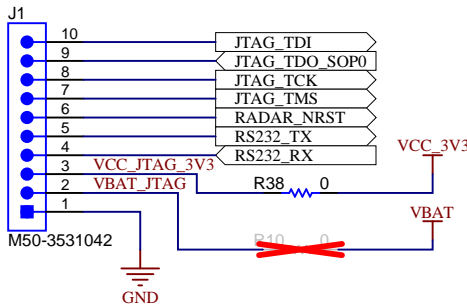
B

CAN_FD_TRANSCEIVER



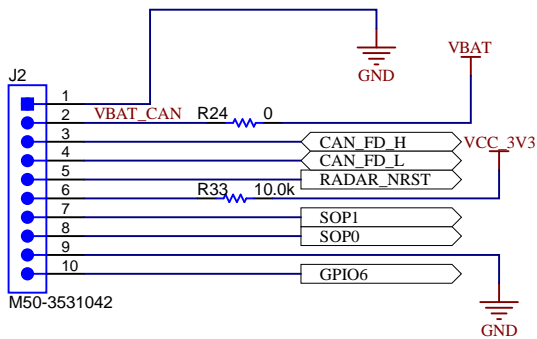
CONNECTORS

JTAG/RS232

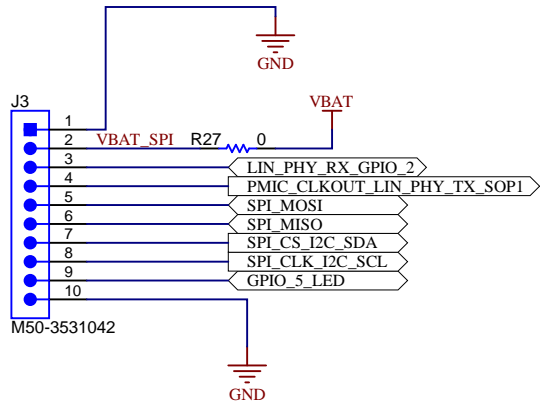


Review Note
since J1.3 is 3.3V source pin, pullup is not added. Please confirm

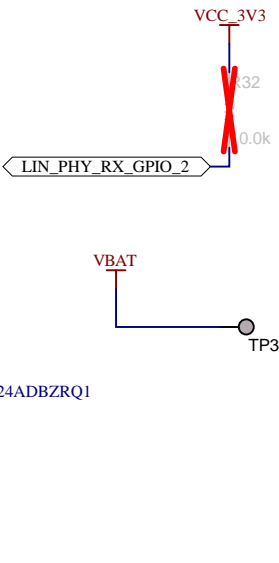
CAN/SOP



SPI/I2C/LIN



Design Note
GPIO_5_LED is used as SPI busy signal.





PCB Number: TIDEP-01037
PCB Rev: A

PCB
LOGO
Texas Instruments



PCB
LOGO
FCC disclaimer

PCB
LOGO
WEEE logo

CAUTION HOT SURFACE1



CAUTION HOT SURFACE

| Variant/Label Table | |
|---------------------|-----------------------------|
| Variant | Label Text |
| 001_AWR | AWRL6432_INCABIN_REF_DESIGN |
| | |

LBL1

PCB Label

THT-14-423-10
Size: 0.65" x 0.20 "

CAPACITORS HIGHLIGHTED IN THE RED COLOR BOXES ARE ADDED FOR IMPROVEMENT AND THOSE ARE NOT MANDITORY.

ZZ1

Label Assembly Note

This Assembly Note is for PCB labels only

ZZ2

Assembly Note

These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3

Assembly Note

These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4

Assembly Note

These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ5

Assembly Note

INDICATION FOR COMPONENTS D* ARE GIVEN AT THEIR CATHODE SIDE.

| | | | | | |
|--|--|---|--|---------------------------------------|---|
| Orderable: AWRL6432InCabinRefDes | | Designed for: Public Release | | Mod. Date: 7/25/2024 | |
| TID #: TIDEP-01037 | | Project Title: AWRL6432_INCABIN_REF_DESIGN | | | |
| Number: TIDEP-01037 | | Rev: A | | Sheet Title: HARDWARE | |
| SVN Rev: 3433 | | Assembly Variant: 001_AWR | | | Sheet: 7 of 7 |
| Drawn By: Mistral | | File: AWRL6432_REF_DESIGN_Hardware.SchDoc Size: B | | | |
| Engineer: Mistral | | Contact: http://www.ti.com/support | | | |

Texas Instruments and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. Texas Instruments and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. Texas Instruments and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.